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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
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U.S. APPLICATION NO. (If known, see 37CFR1.5)	
10/030656	
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE / PRIORITY DATE CLAIMED
PCT/JP00/05624	August 23, 2000 / August 27, 1999

TITLE OF INVENTION
ETCHING METHOD AND PLASMA PROCESSING METHOD

APPLICANT(S) FOR DO/EO/US
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Applicant(s) herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c)(2)).
   a. ☐ is attached hereto (required only if not communicated by the International Bureau.
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed with the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154 (d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☒ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☒ Information Disclosure Statement under 37 CFR 1.97 and 1.98
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A Substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154 (d)(4).
19. ☐ A second copy of the English language translation of the international application 35 U.S.C. 154 (d)(4).
20. ☒ Other items or information:
    a. ☒ Copy of cover page of International Publication No. WO 01/17007
    b. ☐ Copy of Notification of Missing Requirements.
    c. ☐

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/050656	PCT/JP00/05624	07553.0029

21. ☒ The following fees are submitted: — CALCULATIONS PTO USE ONLY

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**

International preliminary examination fee (37 CFR 1.482) paid to USPTOand all claims satisfied provisions of PCT Article 33 (1)-(4) **$100.00**

				ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).					$	
CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE		
Total Claims	11	- 20 =		x $18.00	$	
Independent Claims	2	-3 =		x $84.00	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)				+$280.00	$	
				TOTAL OF THE ABOVE CALCULATIONS =	$890.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.					$	
				SUBTOTAL =	$890.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest priority date (37 CFR 1.492(f)).					$	
				TOTAL NATIONAL FEE =	$890.00	
Fee for recording the enclosed assignment (37 CFR 1.21 (h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property. +					$40.00	
				TOTAL FEES ENCLOSED =	$930.00	
					Amount to be refunded:	$
					charged:	$

a. ☒ A check in the amount of $ 930.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 06-0916. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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DATED: January 11, 2002

DESCRIPTION

Etching Method and Plasma Processing Method

TECHNICAL FIELD

The present invention relates to an etching method and a plasma processing method.

BACKGROUND ART

As ultra high integration in semiconductor devices increasing in recent years, manufacturing superfine metal wirings that conform to rigorous design rules has become a crucial technical requirement. However, when the aluminum wirings normally utilized in the prior art, such as wirings constituted of Al or an Al alloy, are miniaturized, the level of the electrical resistance becomes significant, which readily causes a wiring delay, lowering the operating speed of the semiconductor device. As a solution, adoption of Cu having a lower electrical resistance value than Al as the wiring material has been considered in recent years. However, Cu becomes oxidized more readily than Al. Accordingly, during the semiconductor manufacturing process, a Cu wiring layer is covered with a layer constituted of a material that does not contain O_2, e.g., an SiN_x layer, to prevent oxidation of the Cu wiring layer by assuring that it is not exposed to O_2.

When connecting a Cu wiring to another wiring in a semiconductor device adopting a multilayer wiring structure, it is necessary to to etch the SiN_x layer and to form at the SiN_x layer a connecting hole such as a via hole through which the Cu wiring layer is exposed. However, a CF (fluorocarbon) processing gas containing O_2 is usually utilized in the plasma etching process during which the SiN_x layer is etched. As a result, the surface of the exposed Cu wiring layer becomes oxidized by O_2 or an oxide compound is formed at the

Cu wiring layer during the etching process. Such a reaction product raises the electrical resistance value at the area where the Cu wiring is connected with the other wiring, thereby presenting a problem in that the device characteristics of the semiconductor device are compromised.

An object of the present invention, which has been completed by addressing the problem of the prior art discussed above, is to provide a new and improved etching method and a new and improved plasma processing method that solve the problem above and other problems.

DISCLOSURE OF THE INVENTION

In order to achieve the object described above, in a first aspect of the present invention, an etching method for etching an SiN_x layer present on a Cu layer formed at a workpiece placed in a processing chamber by raising to plasma a processing gas introduced into the processing chamber, which is characterized in that the processing gas contains a gas constituted of C, H and F and O_2, is provided.

In the etching process implemented by using the gas constituted of C, H and F according to the present invention, the exposed surface of the Cu layer is not oxidized readily. In addition, this effect is sustained regardless of whether or not O_2 is present. For this reason, even when a wiring, for instance, is connected at the exposed surface of the Cu layer, the electrical resistance value at the connection area is not raised. Furthermore, by adding O_2 into the gas constituted of C, H and F, it becomes possible to even more effectively prevent the oxidation of the Cu layer.

The gas constituted of C, H and F should be CH_2F_2, CH_3F or CHF_3.

In addition, it is desirable to add an inert gas into the processing gas. When an inert gas is added into the processing gas,

the contents of the gas constituted of C, H and F and O_2 can be adjusted as necessary in correspondence to specific process requirements while maintaining the quantity of the processing gas introduced into the processing chamber at a predetermined level.

Moreover, in a second aspect of the present invention, a plasma processing method comprising a step in which an SiN_x layer is etched by using a photoresist layer having a specific pattern formed therein, a step implemented after the etching step, a step implemented after said etching step, in which said photoresist layer is ashed and a step implemented after said ashing step, in which a plasma process is implemented on the exposed Cu layer by raising to plasma H_2 introduced into the processing chamber is provided.

It is to be noted that the exposed surface of the Cu layer may become oxidized during the ashing step as well. In addition, if a CF gas is used as the processing gas during the etching step, C (carbon atoms) and F (fluorine atoms) may be injected into the exposed surface of the Cu layer. Accordingly, in a third aspect of the present invention, the surface of the Cu layer is treated with H_2 plasma after the etching step and the ashing step to deoxidize the oxidized Cu and to remove C and F. As a result, the electrical resistance value at the connection area where the Cu wiring is connected to the other wiring is prevented from increasing even more effectively.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic sectional view of a plasma processing apparatus in which the present invention may be adopted;

FIG. 2 presents schematic sectional views of a wafer before and after implementing a process by adopting the etching method according to the present invention;

FIG. 3 presents schematic diagrams to facilitate an explanation of an implementation example of the etching method according to the present invention; and

FIG. 4 presents schematic diagrams to facilitate an explanation of the implementation example of the etching method according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The following is a detailed explanation of a preferred embodiment of the etching method and the plasma processing method according to the present invention, given in reference to the attached drawings.

(1) Etching Method

First, the etching method adopted in the embodiment is explained.

(a) Overall Structure of Etching Apparatus

First, in reference to FIG. 1, a brief explanation is given on a plasma processing apparatus 100 that may adopt the etching method achieved in the embodiment. A processing chamber 102 is formed in an airtight processing container 104. A magnet 106 is provided around the processing container 104 so as to form a rotating magnetic field inside the processing chamber 102. In addition, a lower electrode 108 on which a workpiece such as a semiconductor wafer (hereafter referred to as a "wafer") W may be placed is provided inside the processing chamber 102. An upper electrode 110 is provided to face opposite the mounting surface of a lower electrode 108 in the processing chamber 102.

Numerous gas outlet holes 110a are formed at the upper electrode 110. The gas outlet holes 110a are connected with first ~ third gas supply sources 124, 126 and 128 respectively via first ~

third switching valves 112, 114 and 116 and first ~ third flow regulating valves 118, 120 and 122. CH_2F_2, O_2 and Ar constituting the processing gas used in the embodiment are respectively stored in the first ~ third gas supply sources 124, 126 and 128. This structure allows the processing gas constituted of CH_2F_2, O_2 and Ar individually set at predetermined flow rates to be introduced into the processing chamber 102 via the gas outlet holes 110a. It is to be noted that the etching process implemented by using the processing gas is to be detailed later.

In addition, the processing gas introduced into the processing chamber 102 is raised to plasma when high frequency power output from a high frequency source 130 is applied to the lower electrode 108 via a matcher 132. The gas inside the processing chamber 102 is evacuated via a baffle plate 134 provided around the lower electrode 108 and an evacuating pipe 136. It is to be noted that the plasma processing apparatus 100 assumes a structure which allows it to perform an ashing process and a surface treatment on a Cu layer 204 to be detailed later as well as the etching process.

(b) Etching Process

Next, in reference to FIGS. 1 and 2, a detailed explanation is given on the etching process implemented on the wafer W by using the processing gas in the embodiment. It is to be noted that FIG. 2(a) presents a schematic sectional view of the wafer W in the state before an SiN_x layer 206 is etched. FIG. 2(b) presents a schematic sectional view of the wafer W in the state after the SiN_x layer 206 is etched.

As shown in FIG. 2(a), the Cu layer (Cu wiring layer) 204 is formed at a first SiO_2 layer 200 via a TaN layer 202 which functions as a barrier metal layer. In addition, the SiN_x layer 206 which is to undergo the etching process in the embodiment is formed on the Cu layer 204 to prevent the oxidization of the Cu layer 204. A second SiO_2

layer 208 to be used as a layer insulating film and a photoresist layer 210 having a specific pattern formed therein are sequentially laminated over the SiN_x layer 206.

The etching process is implemented in the embodiment after forming a via hole 212 which reaches the SiN_x layer 206 is formed at the second SiO_2 layer 208 through a specific type of etching process as shown in FIG. 2(a). Namely, the processing gas introduced into the processing chamber 102 to etch the second SiO_2 layer 208 is first switched to the processing gas constituted of CH_2F_2, O_2 and Ar which characterizes the embodiment. At this point, the flow rate ratio (CH_2F_2/O_2/Ar) of CH_2F_2, O_2 and Ar is set at, for instance, 10sccm ~ 30sccm / 10sccm ~ 30sccm / 100sccm ~ 200sccm. The pressure inside the processing chamber 102 may be set at, for instance, 30mTorr ~ 100mTorr. Then, high frequency power having a frequency of, for instance, 13.56 MHz and achieving a 300 W ~ 1000 W level is applied to the lower electrode 108.

Such high frequency power application causes the processing gas to dissociate to generate plasma. As a result, the SiN_x layer 206 becomes etched by the plasma and the upper surface of the Cu layer 204 becomes exposed at the bottom of the via hole 212 as shown in FIG. 2(b). Since the SiN_x layer 206 has been etched by using the processing gas constituted of CH_2F_2, O_2 and Ar, the surface of the Cu layer 204 is hardly oxidized during this process, as explained later in reference to subsequent implementation examples.

(c) Implementation Example

Next, an example of actual implementation of the embodiment is explained in reference to FIG. 3 and FIG. 4. It is to be noted that FIGS. 3 (a) and (b) and FIGS. 4 (a) and (b) each schematically illustrate the relationship between the depth measured from the surface of the Cu layer 204 and the content of the elements present in

the Cu layer 204 at the corresponding depth. The Cu layer 204 was gradually etched by spraying Ar at a predetermined pressure on to the exposed surface of the Cu layer 204.

In the implementation example, the SiN_x layer 206 at the wafer W shown in the FIG. 2(a) was etched by employing the plasma processing apparatus 100 explained earlier. The flow rate ratio of the constituents in the processing gas was set at $CH_2F_2/O_2/Ar$ = 20 sccm/10sccm/100sccm. In addition, the pressure inside the processing chamber 102 was set at 50mTorr. High frequency power with a frequency set at 13.56 MHz and achieving a 500 W level was applied to the lower electrode 108. The results presented in FIG. 3(a) were achieved by etching the wafer under the conditions described above. As shown in FIG. 3(a), the Cu layer 204 was hardly oxidized when the process was implemented by using the processing gas constituted of CH_2F_2, O_2 and Ar, with hardly any C and F injection observed. Thus, we may conclude that the processing gas is effective in preventing damage to the Cu layer 204.

Next, as an example that provides a comparison to the implementation example described above, an etching process was implemented by using a processing gas constituted of CF_4 and Ar, and the results presented in FIG. 3(b) were obtained. It is to be noted that the processing gas constituted of CF_4 and Ar is normally used in an etching process implemented on the SiO_2 layer 208 or the SiN_x layer 206. The flow rate ratio of the constituents of the processing gas was set at CF_4/Ar = 20sccm/100sccm. Otherwise, the process was implemented under the same processing conditions as those described above. As shown in FIG. 3(b), when the processing gas constituted of CF_4 and Ar was used, the Cu layer 204 became oxidized to a greater depth and a greater degree of injection of C and F was observed compared to the extent of oxidation and C/F injection

observed in the etching process implemented by using the processing gas constituted of CH_2F_2, O_2 and Ar described earlier. Thus, one may conclude that the Cu layer 204 becomes damaged more readily when the processing gas constituted of CF_4 and Ar is used.

In addition, an etching process was implemented by using a processing gas constituted of CH_2F_2, N_2 and Ar achieved by mixing N_2 instead of O_2, in order to ascertain the extent of the influence of O_2 present in the processing gas, and the results presented in FIG. 4(a) were achieved. It is to be noted that the flow rate ratio of the constituents of the processing gas was set at CH_2F_2/ N_2 /Ar = 20sccm/ 10 sccm/100sccm as in the processing gas constituted of CH_2F_2, O_2 and Ar. The process was implemented by setting the other processing conditions identically to those described earlier. As shown in FIG. 4(a), the Cu layer 204 became oxidized to an even further depth and a greater degree of C/F injection was observed when the processing gas constituted of CH_2F_2, N_2 and Ar was used compared to the extent of the oxidation and the C/F injection observed in the process implemented by using the processing gas constituted of CH_2F_2, O_2 and Ar and the process implemented by using the processing gas constituted of CF_4 and Ar. This demonstrates that the presence of O_2 in the processing gas constituted of CH_2F_2, O_2 and Ar does not adversely affect the Cu layer 204 but rather, it effectively protects the Cu layer 204.

It is to be noted that the results presented in FIG. 4(b) were achieved by performing a similar measurement on the Cu layer 204 exposed to the atmosphere without implementing the etching process.

As described above, by etching the SiN_x layer 206 covering the Cu layer 204 with the plasma generated from the processing gas constituted of CH_2F_2, O_2 and Ar, it is possible to minimize the extent of oxidation of the exposed Cu layer 204 and to reduce the extent to

which C and F constituting the CH_2F_2 are injected into the Cu layer 204. As a result, the electrical resistance value at the connection area does not increase even when another wiring is connected to the exposed surface of the Cu layer 204.

(2) Ashing Method

Next, a method that may be adopted to implement an ashing process on the photoresist layer 210 formed at the wafer W is explained. During the process for manufacturing a semiconductor device, an ashing process is normally implemented after the etching process to remove the photoresist layer 210 used as an etching mask. However, there is a risk of the Cu layer 204 which has not been oxidized during the etching process becoming oxidized during the ashing process implemented by adopting the method in the prior art. Accordingly, it is desirable to implement an ashing process through the following method on the wafer W that includes the Cu layer 204.

Namely, following the etching process described above, the temperature of the wafer W remaining on the lower electrode 108 is sustained at 100°C or lower and preferably at 40°C. The temperature of the wafer W is adjusted by a temperature control mechanism (not shown) internally provided at the lower electrode 108. In addition, a processing gas constituted of, for instance, O_2, is introduced into the processing chamber 102 at a flow rate of 200sccm. Then, high frequency power with a frequency of 13.56 MHz and achieving a level of 1000 W is applied to the lower electrode 108. Through this power application, the processing gas is raised to plasma and thus, the photoresist layer 210 at the wafer W shown in FIG. 2(b) is removed.

In this method, the ashing process is implemented while sustaining the temperature of the wafer W at 100°C or lower and, as a result, the degree to which the Cu layer 204 is oxidized is minimized.

Thus, the state of the Cu layer 204 after the ashing process remains essentially unchanged from the state following the etching process.

(3) Method of Treating Surface of Cu Layer (H_2 Plasma Process)

Next, a method that may be adopted to treat the surface of the Cu layer 204 is explained. It is difficult to completely prevent the oxidation of the Cu layer 204 and the entry of C and F even when the process is implemented by adopting the etching method and the ashing method described above. Accordingly, it is desirable to implement the following surface treatment on the Cu layer 204.

Namely, after the etching process and the ashing process described above, the processing gas introduced into the processing chamber 102 is switched to H_2 with the wafer W still remaining inside the processing chamber 102. The flow rate of H_2 may be set at, for instance, 200sccm. In addition, the pressure inside the processing chamber 102 may be set at, for instance, 50mTorr. Then, H_2 plasma is generated inside the processing chamber 102 by applying 1000 W high frequency power with its frequency set at, for instance, 13.56 MHz to the lower electrode 108. The H_2 plasma thus generated deoxidizes the Cu layer 204 which has been oxidized. At the same time, the Cu layer 204 is subject to ion implant, which eliminates C and F having been injected into the Cu layer 204 during the etching process. As a result, a Cu layer 204 which does not contain O (oxygen atoms), C and F can be formed.

In addition, the relationship between the depth measured from the surface of the Cu layer 204 and the contents of O, C and F contained in the Cu layer 204 at the corresponding depth was ascertained with regard to the Cu layer 204 before and after the H_2 plasma process. The results indicate that the contents of O, C and F up to 30Å from the surface of the Cu layer 204 became greatly reduced after the process.

Furthermore, the surface of the Cu layer 204 can be treated by utilizing the plasma processing apparatus 100 employed to implement the etching process and the ashing process when the method described above is adopted. This means that the surface of the Cu layer 204 does not need to be treated by employing another processing apparatus. Thus, the individual processes can be continuously performed on the plasma processing apparatus 100 to achieve an improvement in the throughput and a reduction in the production costs.

While the invention has been particularly shown and described with respect to the preferred embodiment thereof by referring to the attached drawings, the present invention is not limited to these examples and it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit, scope and teaching of the invention.

For instance, while an explanation is given above in reference to the embodiment on an example in which CH_2F_2 is used as a constituent of the etching processing gas, the present invention is not limited to this example and the advantages described above may be achieved by using CH_2F_2, CH_3F or CHF_3 instead of CH_2F_2.

In addition, while an explanation is given above in reference to the embodiment on an example in which Ar is added into the etching processing gas, the present invention is not limited to this example and it may be effectively implemented by using an inert gas such as He instead of Ar or without adding any inert gas.

While an explanation is given above in reference to the embodiment on an example in which a single plasma processing apparatus is utilized to implement the etching process, the ashing process and the Cu layer surface treatment, the present invention is not limited to this example and it may be also adopted when separate

plasma processing apparatuses are employed to perform the individual processes described above.

According to the present invention, the SiN_x layer formed on the Cu layer can be etched, while minimizing the extent to which other elements become mixed in the Cu layer. In addition, other elements present in the Cu layer can be eliminated through the plasma process implemented by using H_2. As a result any degradation of the Cu layer can be prevented.

INDUSTRIAL APPLICABILITY

As explained above, the present invention may be adopted during the process of manufacturing semiconductor devices and, in particular, it is ideal in an application in which a plasma process such as etching is implemented on an SiN_x layer formed on a Cu layer.

Scope of Amended Claims

["Received at International Office on January 14, 2001 (14. 01. 01): Claims 1 and 6 in the initial application have been amended; no amendments in other claims (2 pages)]

1. (amended) An etching method for etching an SiN_x layer on a Cu layer formed at a workpiece placed inside a processing chamber by raising to plasma a processing gas introduced into said processing chamber to expose said Cu layer, wherein;

said processing gas contains a gas constituted of C, H and F and O_2.

2. An etching method according to claim 1, wherein;
said gas constituted of C, H and F is CH_2F_2.

3. An etching method according to claim 1, wherein;
said gas constituted of C, H and F is CH_3F.

4. An etching method according to claim 1, wherein;
said gas constituted of C, H and F is CHF_3.

5. An etching method according to claim 1, wherein;
an inert gas is added into said processing gas.

6. (amended) A plasma processing method comprising;

a step in which a processing gas containing a gas constituted of C, H and F and O_2 is raised to plasma and an SIN_X layer on a Cu layer is etched using a photoresist layer having a specific pattern formed therein, thereby exposing said Cu layer;

a step implemented after said etching step, in which said photoresist layer is ashed; and

a step implemented after said ashing step, in which H_2 is introduced into said processing chamber and an H_2 plasma process is implemented on said Cu layer that has become exposed by raising the H_2 to plasma.

7. An etching method according to claim 6, wherein;
said gas constituted of C, H and F is CH_2F_2.

8. An etching method according to claim 6, wherein;
said gas constituted of C, H and F is CH_3F.

9. An etching method according to claim 6, wherein;
said gas constituted of C, H and F is CHF_3.

10. An etching method according to claim 6, wherein;
an inert gas is added into said processing gas.

11. An etching method according to claim 6, wherein;
said etching step, said ashing step and said H_2 etching step are implemented inside a single processing chamber.

Argument based upon Treaty Article 19 (1)

While a technology similar to that achieved in the invention is disclosed in Japanese Unexamined Patent Publication No. H 5-16077 (quoted reference), the quoted reference does not describe the feature that characterizes the invention, i.e., the etching process implemented on the SiN_x layer formed on the Cu layer, and it does not disclose in any way whatsoever another feature of the invention that by adding O_2 into the etching gas, the exposed Cu layer is protected to inhibit the process of oxidation, either. In addition, even by combining the technology disclosed in another quoted reference with the technology disclosed in the quoted reference mentioned above, a person skilled in the art cannot achieve the invention with ease. We are convinced that the invention, which adopts the structural features listed above, is patentable over the entire scope of patent claims set forth herein.

Explanation of Reference Numerals

100 plasma processing apparatus
102 processing chamber
104 processing container
106 magnet
108 lower electrode
110 upper electrode
110a gas outlet hole
112, 114, 116 first ~ third switching valves
118, 120, 122 first ~ third flow regulating valves
124, 126, 128 first ~ third gas supply sources
130 high frequency source
132 matcher
134 baffle plate
136 evacuating pipe
200 first SiO_2 layer
204 Cu layer
206 SiN_x layer
208 second SiO_2 layer
210 photoresist layer
W wafer

FIG.1

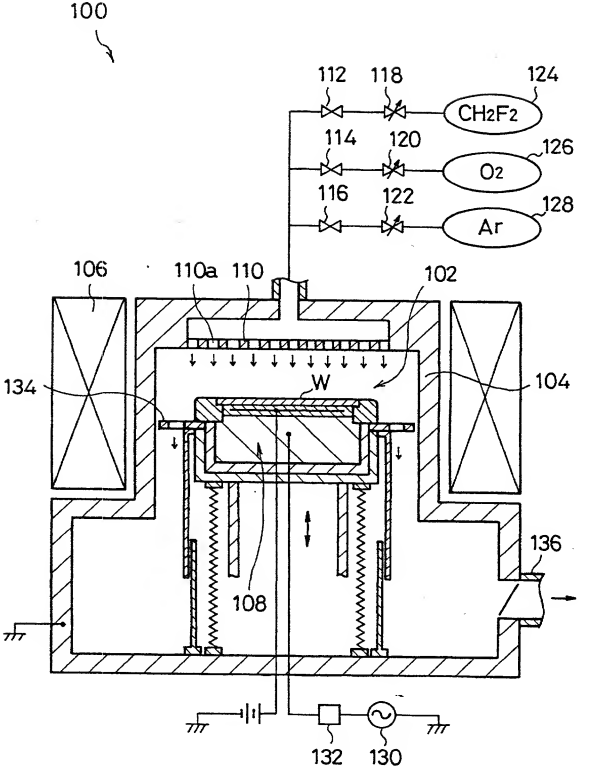


FIG.2(a)

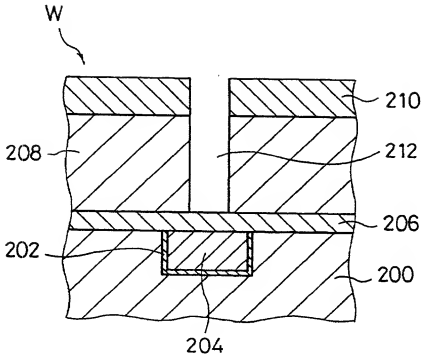


FIG.2(b)

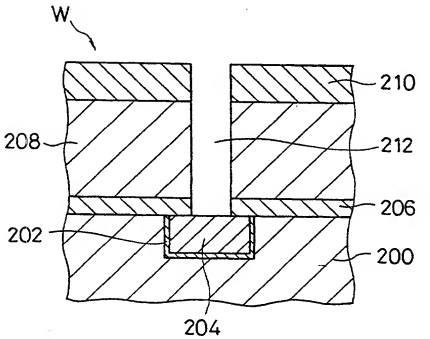


FIG.3(a)

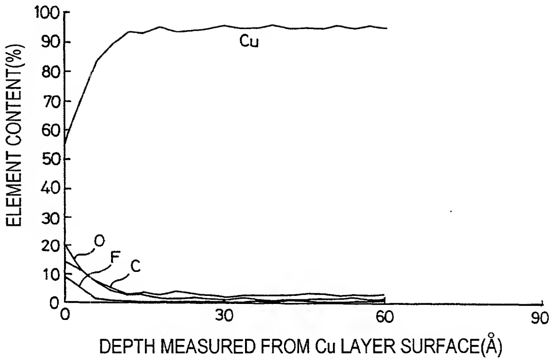


FIG.3(b)

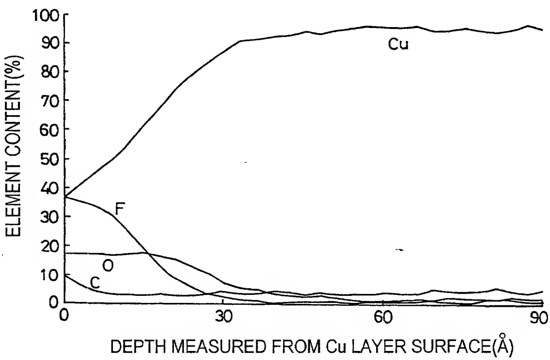


FIG.4(a)

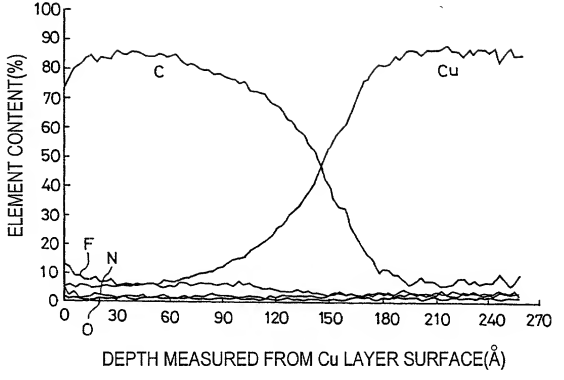
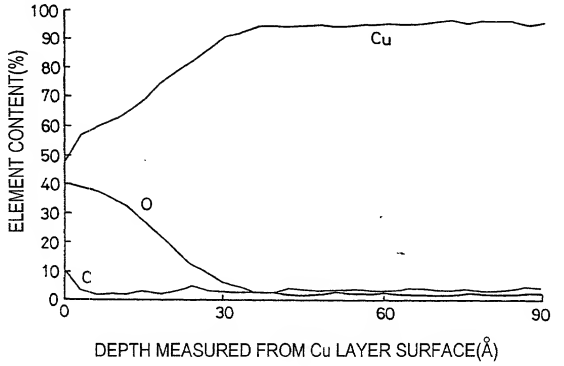


FIG.4(b)



Attorney Docket No. _____

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: Etching Method and Plasma Processing Method

the specification of which ☐ is attached and/or ☒ was filed as United States Application Serial No. _____ on _____ and was amended on _____ (if applicable); or was filed as PCT International Application No. PCT/JP00/05624 on August 23, 2000 and was amended on January 14, 2001 (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Country	Application Number	Date of Filing	Priority Claimed Under 35 U.S.C. 119
Japan	JP11-241427	August 27, 1999	☒ YES ☐ NO
PCT	PCT/JP00/05624	August 23, 2000	☒ YES ☐ NO

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	Date of Filing	Status (Patented, Pending, Abandoned)

I hereby appoint the following attorney and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. **FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P., Reg. No. 22,540,** Douglas B. Henderson, Reg. No. 20,291; Ford F. Farabow, Jr., Reg. No. 20,630; Arthur S. Garrett, Reg. No. 20,338; Donald R. Dunner, Reg. No. 19,073; Brian G. Brunsvold, Reg. No. 22,593; Tipton D. Jennings, IV, Reg. No. 20,645; Jerry D. Voight, Reg. No. 23,020; Laurence R. Hefter, Reg. No. 20,827; Kenneth E. Payne, Reg. No. 23,098; Herbert H. Mintz, Reg. No. 26,691; C. Larry O'Rourke, Reg. No. 26,014; Albert J. Santorelli, Reg. No. 22,610; Michael C. Elmer, Reg. No. 25,857; Richard H. Smith, Reg. No. 20,609; Stephen L. Peterson, Reg. No. 26,325; John M. Romary, Reg. No. 26,331; Bruce C. Zotter, Reg. No. 27,680; Dennis P. O'Reilley, Reg. No. 27,932; Allen M. Sokal, Reg. No. 26,695; Robert D. Bajefsky, Reg. No. 25,387; Richard L. Stroup, Reg. No. 28,478; David W. Hill, Reg. No. 28,220; Thomas L. Irving, Reg. No. 28,619; Charles E. Lipsey, Reg. No. 28,165; Thomas W. Winland, Reg. No. 27,605; Basil J. Lewris, Reg. No. 28,818; Martin I. Fuchs, Reg. No. 28,508; E. Robert Yoches, Reg. No. 30,120; Barry W. Graham, Reg. No. 29,924; Susan Haberman Griffen, Reg. No. 30,907; Richard B. Racine, Reg. No. 30,415; Thomas H. Jenkins, Reg. No. 30,857; Robert E. Converse, Jr., Reg. No. 27,432; Clair X. Mullen, Jr., Reg. No. 20,348; Christopher P. Foley, Reg. No. 31,354; John C. Paul, Reg. No. 30,413; Roger D. Taylor, Reg. No. 28,992; David M. Kelly, Reg. No. 30,953; Kenneth J. Meyers, Reg. No. 25,146; Carol P. Einaudi, Reg. No. 32,220; Walter Y. Boyd, Jr., Reg. No. 31,738; Steven M. Anzalone, Reg. No. 32,095; Jean B. Fordis, Reg. No. 32,984; Barbara C. McCurdy, Reg. No. 32,120; James K. Hammond, Reg. No. 31,964; Richard V. Burgujian, Reg. No. 31,744; J. Michael Jakes, Reg. No. 32,824; and _____. Please address all correspondence to **FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER,** L.L.P. 1300 I Street, N.W., Washington, D.C. 20005, Telephone No. (202) 408-4000.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Attorney Docket No. _____

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